Notice of Allowability	Application No.	Applicant(s)	
	09/965,033	WONG, YU	
	Examiner	Art Unit	
	Leo Boutsikaris	2872	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed on 9/5/02*.

2. ☒ The allowed claim(s) is/are *1-12*.

3. ☒ The drawings filed on *25 September 2001* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Bing Ai (Reg. No. 43,312) on 5/12/2005.

The application has been amended as follows:

IN THE CLAIMS

Claim 1 is rewritten as follows:

1. A device, comprising:

a plurality of layers stacked over one another to form a layered structure which supports a two-dimensional array of light-filtering channels, wherein each layer is structured to have an one-dimensional array of light-filtering channels,

[an] wherein the two-dimensional array of light-filtering channels [having] comprises an input surface from which said light-filtering channels receive input light and an output surface from which said light-filtering channels export output light, and wherein each light-filtering channel comprises:

a light-conducting channel formed of a transparent dielectric material having a first surface which is substantially reflective and a second surface opposing said first

surface, said first and second surfaces substantially parallel to said light-conducting channel; and

at least two optical filters sequentially formed on said second surface along said light-conducting channel to reflect said input light between said first and second surfaces so that said input light is sequentially reflected and filtered by said optical filters to produce said output light, wherein each optical filter includes at least one metal layer and an electro-optical dielectric layer contacting with each other to form a metal-dielectric interface which generates a surface plasmon wave in response to a p-polarized input light beam to transmit light at a selected wavelength within a bandwidth according to a control voltage from said metal layer to said dielectric layer and reflects light of other wavelengths; and

at least two thin-film transistors respectively formed on said optical filters to provide said control voltage to control a refractive index of said dielectric layer and thereby said selected wavelength to change a color and a gray scale of said output light.

Claim 6 is rewritten as follows:

6. A device, comprising:

a plurality of transparent plates each having a filtering surface and an opposing, reflecting surface, a metallic layer formed over said filtering surface of each transparent plate;

an electro-optical dielectric layer, whose refractive index changes in response to a control voltage, disposed in contact with said metallic layer to form a metal-dielectric interface which generates a surface plasmon wave in response to a [p-polarized] <u>polarized</u>

input light beam to transmit light through said metallic layer at a selected wavelength within a bandwidth according to a local refractive index of said electro-optical dielectric layer at each location of said metallic layer where light is reflected and to reflect light of other wavelengths back to each transparent plate; and

a plurality of parallel linear arrays of transistors formed over said dielectric layer, wherein said transistors are independent from one another, and where each parallel linear array of transistors defines a light channel along which light is reflected between said filtering and said reflecting surfaces via at least two locations on the filtering surface with two transistors sequentially located along the light channel to modify a color and an intensity of said light according to voltages from said transistors in each linear array relative to a common voltage of said metallic layer,

wherein said transparent plates are stacked over one another so that a reflecting surface of one transparent plate faces a filtering surface of an adjacent transparent plate to form a two-dimensional array of light channels.

Claims 11-16 are cancelled.

The following new claims are added:

17. (New) A method, comprising:

providing a plurality of plates each comprising a dielectric material layer having a first reflective surface and a second, opposing metallic surface;

patterning the second metallic surface to include a two-dimensional array of separate metallic areas, a plurality of metal-dielectric interfaces on each separate metallic

area, and thin-film transistors above the metal-dielectric interfaces respectively on the separate metallic areas;

stacking and bonding the plates over one another to form a composite structure; and

slicing the composite structure into a plurality of panels of two-dimensional light-filtering channels where each panel includes a portion of the stacked plates and each portion in each plate includes at least three separate metallic areas as three independent surface filters along a direction that is perpendicular to a direction of the slicing and defines a light-filtering channel wherein light incident to one of the light-filtering channels of the plate is sequentially reflected and filtered by the three surface plasmon filters to produce a filtered optical output on the side of the plate.

18. (New) The method as in claim 17, further comprising:

providing independent electric controls to separate metallic areas in one sliced panel; and

controlling voltages applied to the independent electrical controls to control light intensities and colors of output light from the light-filtering channels for light entering from one side of the panel and exiting on an opposite side of the panel.

The following is an examiner's statement of reasons for allowance:

Claims 1-10, 17-18 are allowable over the prior art of record for at least the reason that even though the prior art discloses a color display panel comprising a metal/dielectric interface for filtering incident light, the prior art fails to teach or

reasonably suggest, regarding claims 1-5, a device comprising at least two optical filters sequentially formed on the second surface along the light-conducting channel to reflect the input light between the first and second surfaces so that the input light is sequentially reflected and filtered by the optical filters, wherein each optical filter includes a metal-dielectric interface which generates a surface plasmon wave, regarding claims 6-10, a device wherein each parallel linear array of transistors defines a light channel along which light is reflected between the filtering and reflecting surfaces via at least two locations on the filtering surface with two transistors sequentially located along the light channel, and regarding claims 17-18, a method wherein light incident to one of the light-filtering channels of the plate is sequentially reflected and filtered by the three surface plasmon filters to produce a filtered optical output on the side of the plate, as set forth by the claimed combination.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Leo Boutsikaris whose telephone number is 571-272-2308.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Leo Boutsikaris, Ph.D., J.D.
Primary Patent Examiner, AU 2872
May 13, 2005

LB

LEONIDAS BOUTSIKARIS
PRIMARY EXAMINER